DWG ISSUE	EE OR CD ISSUED	DATE ISSUE		APPD
1	—	10/4/74	LRE LRE	RWF MTS RFG
2A1	—	9-8-76	P/S LRE	CE LEG RFG
3D1		11-21-77	GC TLB	CE DAH MG

SHEET INDEX

CONTENTS	SHEET NO.	SHEET ISSUE
SHEET INDEX SYMBOL RECORD OF CHANGES NOTES USED-ON TABLE SUPPORTING INFORMATION CURRENT DRAIN	1	3
CIRCUIT SCHEMATIC	2	3
COMPONENT LIST CIRCUIT DESCRIPTION	3	3

RECORD OF CHANGES

DWG ISS	PREV FURN	STD	MFR DISC	SEE NOTE
2A1	Z	Y	Z	

SYMBOL

BUFFER D
ELEMENT IDENT
A

TERM. MOD	FUNCT	TERM.	LOC
CLC01	I	012	2A0
CLC11	I	115	2A7
1ACTO	I	116	2A3
LOD0	I	014	2A4
∅FLCLX1	I	210	2A2
∅NLCLKD	I	309	2A2
SDIN0	I	015	2A3
-17.20V	I	018,117	2A6
BACR0	∅	TD7	2H5
BA16CRO	∅	006	2H2
IBCC1	∅	013	2H5
I16BC1	∅	016	2H3
SDITR0	∅	1*4	2H6
SD∅TO	∅	208	2H7
(Z) -12V	∅	218	2A6
+5	P	000,119	2H0
GRD	G	200,319	2H2

SYSTEM USED ON	DESIGN CONTROL
COMMON SYSTEMS	IH

CURRENT DRAIN: +5V SUPPLY = 550mA
-17.2V SUPPLY = 50mA (Z)

NOTES:

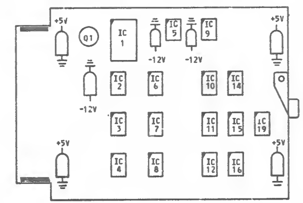
1. ⏚ GROUND RETURN
2. UNLESS OTHERWISE SPECIFIED:
   RESISTANCE VALUES ARE IN OHMS
   CAPACITANCE VALUES ARE IN MICROFARADS
   VALUES PRECEDED BY THE SYMBOL +(PLUS) OR -(MINUS) ARE IN VOLTS
3. BATTERY AND GROUND TERMINALS FOR INTEGRATED CIRCUITS

IC CODE	BAT. TERM.	GRD TERM.
41AC	16	7,8
41BP	16	8
41CA	16	e
41CJ	16	8
41W	16	8
535K	1,2	5
(Z) 33550C	8	4
KS-21678,L1	16	8
(Y) 2B33B	8	4

4. BATTERY AND GROUND TERMINALS FOR THIS CIRCUIT PACK ARE AS FOLLOWS:

FUNCTION	TERMINAL
+5	000,119
GRD	200,319

5. HORIZONTAL MOUNTING CENTERS AT 1.0 INCH.
6. INTEGRATED CIRCUIT AND TRANSISTOR LOCATION GUIDE: (COMPONENT SIDE SHOWN)



UNMARKED COMPONENTS ARE FILTER CAPACITORS

SUPPORTING INFORMATION

CATEGORY	NO.
CIRCUIT PACK CODE	JK13
CONNECTOR ON FRAME	947C OR 947A
SERIES FOR LATEST CLASS A CHANGE. (ANY HIGHER SERIES IS ACCEPTABLE.)	
ACCEPTABLE SERIES	1,2

SHEET INDEX NOTES

1. WHEN CHANGES ARE MADE IN THIS DRAWING ONLY THOSE SHEETS AFFECTED WILL BE REISSUED.
2. THIS SHEET INDEX WILL BE REISSUED AND BROUGHT UP TO DATE EACH TIME ANY SHEET OF THE DRAWING IS REISSUED, OR A NEW SHEET IS ADDED.
3. THE ISSUE NUMBER ASSIGNED TO A CHANGED OR NEW SHEET WILL BE THE SAME ISSUE NUMBER AS THAT OF THE FIRST SHEET.
4. SHEETS THAT ARE NOT CHANGED WILL RETAIN THEIR EXISTING ISSUE NUMBER.
5. THE LAST ISSUE NUMBER OF THE FIRST SHEET INDEX IS RECOGNIZED AS THE LATEST ISSUE NUMBER OF THE DRAWING AS A WHOLE.

ISSUE 3D1

1N98

AT&CO STANDARD

JK13 CIRCUIT PACK

BUFFER D CIRCUIT

(2)

CPS-JK13
3 SHEETS

BELL TELEPHONE LABORATORIES INCORPORATED

6S

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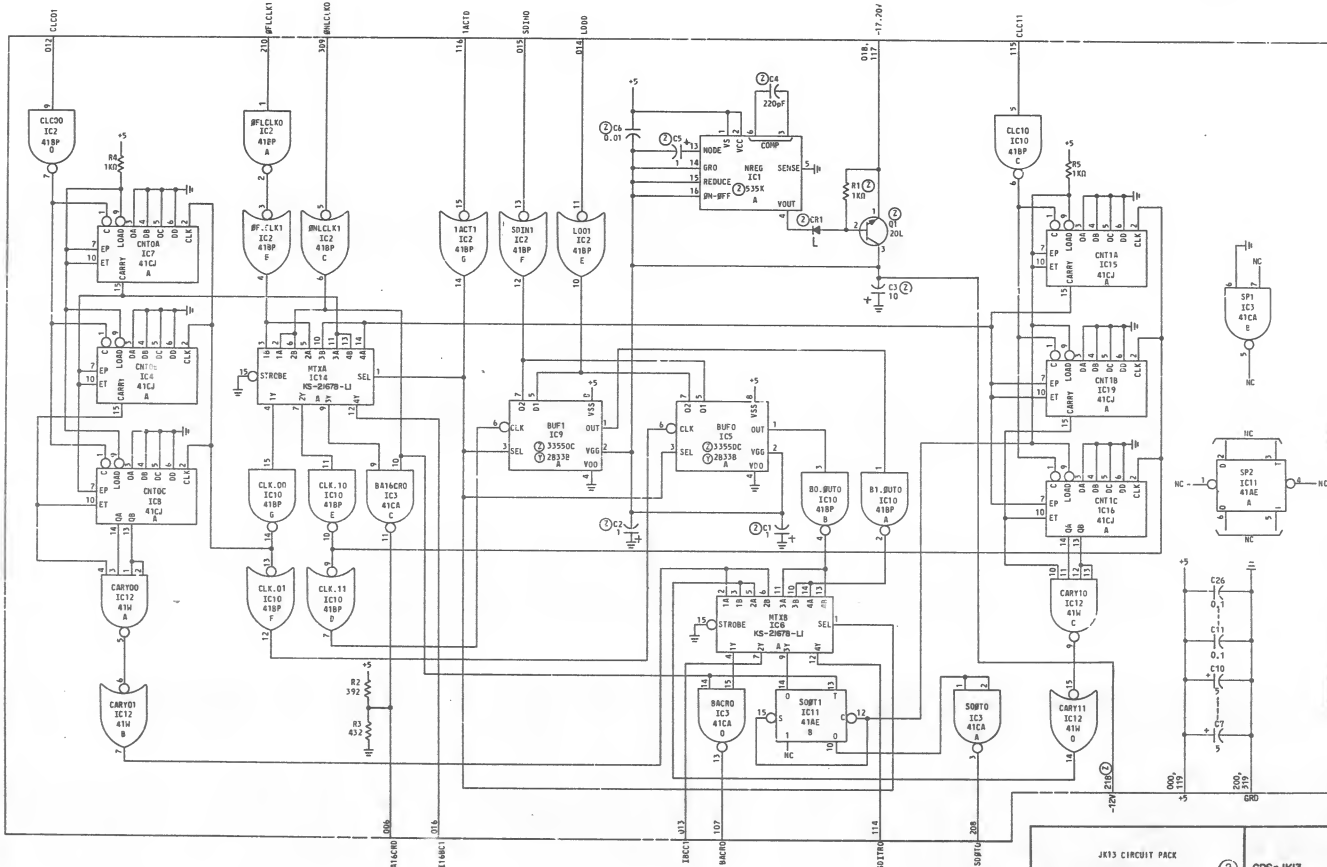
CPS-JK13

PART OF CPS JK13

BUFFER 0



CLC01
ØFLCLK1
ØNLCLK0
1ACTO
SDINO
LODO
-17.20V
CLC11
CLC00 IC2 41BP
ØFLCLK0 IC2 41BP A
ØF.CLK1 IC2 41BP F
ØNLCLK1 IC2 41BP C
1ACT1 IC2 41BP G
SDIN1 IC2 41BP F
LOD1 IC2 41BP E
CNT0A IC7 41CJ A
CNT0B IC4 41CJ A
CNT0C IC8 41CJ A
MTXA IC14 KS-21678-L1
BUF1 IC9 3355OC 2833B A
BUF0 IC5 3355OC 2833B A
NREG IC1 535K A
CLK.00 IC10 41BP G
CLK.10 IC10 41BP E
BA16CR0 IC3 41CA C
CLK.01 IC10 41BP F
CLK.11 IC10 41BP D
CARY00 IC12 41W A
CARY01 IC12 41W B
B0.ØUTO IC10 41BP B
B1.ØUTO IC10 41BP A
MTXB IC6 KS-21678-L1
BACR0 IC3 41CA D
SOØT1 IC11 41AE B
SOØT0 IC3 41CA A
CLC10 IC10 41BP C
CNT1A IC15 41CJ A
CNT1B IC19 41CJ A
CNT1C IC16 41CJ A
CARY10 IC12 41W C
CARY11 IC12 41W D
SP1 IC3 41CA B
SP2 IC11 41AE A
R4 1KΩ
R5 1KΩ
R1 1KΩ
R2 392
R3 432
C4 220pF
C6 0.01
C5
C3 10
C2
C1
Q1 20L
CR1
C26 0.1
C11 0.1
C10 5
C7 5
BA16CR0
I16BC1
I8CC1
BACR0
SDITR0
SDØT0
-12V
+5
GRD

JK13 CIRCUIT PACK

CPS-JK13

SHEET 2

ISSUE 3D1

BELL TELEPHONE LABORATORIES INCORPORATED

6S

CPS-JK13

PART OF CPS JK13

BUFFER 0

COMPONENT LIST

INTEGRATED CIRCUIT

LOC	IC1	IC2	IC3	IC4	IC5	IC6	IC7	IC8	IC9
CODE	535K (2)	41BP	41CA	41CJ	3359DC (FAIRCHILD) (2) 2833B (SYNERTEK) (1)	KS-21678,L1 ~~54157-1-1~~	41CJ	41CJ	3359DC (FAIRCHILD) (2) 2833B (SYNERTEX) (1)
ELEM ID	DESIG / SH LOC	DESIG / SH LOC	DESIG / SH LOC	DESIG / SH LOC	DESIG / SH LOC	DESIG / SH LOC	DESIG / SH LOC	DESIG / SH LOC	DESIG / SH LOC
A	NREG 2B5	@FLCLKD 2B2	SD@T0 2G7	CN10B 2D1	BUFD 2D5	MTKB 2F5	CNT0A 2C1	CNT0C 2E1	BUF1 2D4
B		@F.CLK1 2C2	SP1 2D9						
C		@WLCLK1 2C2	BA16CR9 2E2						
D		CLCD0 2B0	BACR0 2G5						
E		LDD1 2C4							
F		SDIN1 2L3							
G		1ACT1 2C3							

LOC	IC10	IC11	IC12	IC14	IC15	IC16	IC19
CODE	41BP	41AE	41W	KS-21678,L1 ~~54157-1-1~~	41CJ	41CJ	41CJ
ELEM ID	DESIG / SH LOC	DESIG / SH LOC	DESIG / SH LOC	DESIG / SH LOC	DESIG / SH LOC	DESIG / SH LOC	DESIG / SH LOC
A	B1.@UT0 2E6	SP2 2E9	CARY0D 2F1	MTKA 2D2	CNT1A 2C8	CNT1C 2E8	CNT1B 2D8
B	B0.@UT0 2E6	SD@T1 2G5	CARY01 2G1				
C	CLK10 2B7		CARY10 2F7				
D	CLK.11 2F1		CARY11 2G7				
E	CLK.10 2E2						
F	CLK.D1 2F2						
G	CLK.D0 2E2						

CAPACITOR

	DESIG	CODE
[2]	C1,C2	(2) 60DA,1
	C3	(2) 60AA,1D
	C4	(2) KS-19774 L1,220pF
	C5	(2) 60DA,1
	C6	(2) KS-19774 L1,0.01
[4]	C7-C10	60IA,5
[16]	C11-C26	KS-19774 L5,0.1

DIODE

DESIG	CODE
CR1	(2) 446N

RESISTOR

DESIG	CODE
R1	(2) KS-20616 L1A,1KΩ
R2	392
R3	432
R4	1KΩ
R5	KS-20616 L1A,1KΩ

TRANSISTOR

DESIG	CODE
Q1	(2) 20L

CIRCUIT DESCRIPTION:

THIS CIRCUIT PACK IS PART OF THE BUFFER UNIT. TWO 1024-BIT SHIFT REGISTERS, BUFO AND BUF1 PROVIDE SERIAL DATA STORAGE. EACH SHIFT REGISTER HAS ASSOCIATED WITH IT A 10-BIT COUNTER. THE COUNTERS INCREMENT EACH TIME THAT THE ASSOCIATED BUFFER IS CLOCKED. THE TWO BUFFERS CAN BE INDEPENDENTLY CLOCKED DUE TO THE MULTIPLEXING OF CLOCK AND DATA INPUT SIGNALS.

WHEN LEAD 1ACTO IS LOW, BUF1 IS CONSIDERED TO BE ON-LINE AND BUFO IS CONSIDERED TO BE OFF-LINE. ON-LINE CLOCK PULSES AT INPUT @WLCLKO ARE ROUTED THROUGH MTKA AND SHIFT THE DATA @N LEAD SDINO INTO BUF1'S DATA PORT D2. THE SELECT LEAD SEL @N BUF1 IS HIGH AND THE DATA AT BUF1S DATA INPUT PORT D1 IS IGNORED. THE OUTPUT DATA OF BUF1 IS ROUTED THROUGH MTKB AND F/F SOUT1 AND APPEARS @N LEAD SD@T0.

BUF1 IS CLOCKED ON THE TRAILING EDGE OF THE PULSE @N LEAD @WLCLKO AND F/F SOUT1 IS CLOCKED ON THE LEADING EDGE. THE 1024-BIT CARRY OF COUNTER 1 IS ROUTED THROUGH MTKB AND APPEAR @N BACRO. THE 16-BIT CARRY OF COUNTER 1 APPEARS @N LEAD BA16CRO. BA16CRO AND BACRO ARE GATED WITH THE @N-LINE CLOCK PULSE AND THEREFORE ARE AS WIDE AS THE GROUND LEVEL PULSE @N LEAD @WLCLKO.

AS LONG AS LEAD 1ACTO IS AT GROUND LEVEL, BUFO IS CONSIDERED TO BE OFF-LINE. OFF-LINE CLOCK PULSES @N LEAD @FLCLK1 ARE ROUTED THROUGH MTXA AND SHIFT THE DATA @N LEAD LDDO INTO BUFOS DATA INPUT PORT D2. THE SELECT LEAD SEL @N BUFO IS HIGH AND THE DATA AT BUFOS DATA INPUT PORT D1 IS IGNORED. THE OUTPUT DATA OF BUFO IS ROUTED THROUGH MTKB AND APPEARS @N LEAD SD1T0. THE 1024-BIT CARRY OF COUNTER 0 IS ROUTED THROUGH MTKB AND APPEARS @N LEAD 1BCC1. THE 16-BIT CARRY OF COUNTER D IS ROUTED THROUGH MTXA AND APPEARS @N LEAD 1A6BC1.

WHEN LEAD 1ACTO IS HIGH, BUFO IS @N-LINE AND BUF1 IS OFF-LINE. IN THIS STATE @N-LINE CLOCK PULSES SHIFT THE DATA @N LEAD SDINO INTO BUFO AND OFF-LINE CLOCK PULSES SHIFT THE DATA @N LEAD LDDO INTO BUF1.

A HIGH LEVEL @N LEADS CLCD1 AND CLC11 CLEARS COUNTERS CNTO AND CNT1 RESPECTIVELY. THE CLEAR FUNCTION OVERRIDES THE COUNTERS CLOCK INPUTS. AS LONG AS CLEAR IS ACTIVE, ANY CLOCK PULSES TO THE COUNTER ARE IGNORED.

NREG AND TRANSISTOR Q1 PROVIDE A -12V REGULATED SUPPLY VOLTAGE FOR THE MOS SHIFT REGISTERS BUFO AND BUF1 ON SERIES 1 CIRCUIT PACKS.

ISSUE 3D1

JK13 CIRCUIT PACK (2) CPS-JK13 SHEET 3

BELL TELEPHONE LABORATORIES INCORPORATED 6S

CPS-JK13